Notice of Allowability	Application No.	Applicant(s)	
	10/709,293	ALLEN ET AL.	
	Examiner	Art Unit	
	Suchin Parihar	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *application filed on 4/27/2004, amendment filed on 8/4/2006*.

2. ☒ The allowed claim(s) is/are *4;6,7,10-13,18 and 20*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Paul Dinh

PAUL DINH
PRIMARY EXAMINER

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Frederick W. Gibb (Reg. # 37,629) on 9/1/2006.

The application has been amended as follows:

In the claims

In claim 4, between lines 9 and 10, insert:

- -predicting yield of integrated circuit devices produced from said integrated circuit design based on said critical area,- -

In claim 6, between lines 9 and 10, insert:

- -predicting yield of integrated circuit devices produced from said integrated circuit design based on said critical area,- -

In claim 7, between lines 9 and 10, insert:

- -predicting yield of integrated circuit devices produced from said integrated circuit design based on said critical area,- -

In claim 10, between lines 9 and 10, insert:

- -predicting yield of integrated circuit devices produced from said integrated circuit design based on said critical area,- -

In claim 11, between lines 9 and 10, insert:

- -predicting yield of integrated circuit devices produced from said integrated circuit design based on said critical area,- -

In claim 12, between lines 9 and 10, insert:

- -predicting yield of integrated circuit devices produced from said integrated circuit design based on said critical area,- -

In claim 13, between lines 9 and 10, insert:

- -predicting yield of integrated circuit devices produced from said integrated circuit design based on said critical area,- -

In claim 18, between lines 10 and 11, insert:

- -predicting yield of integrated circuit devices produced from said integrated circuit design based on said critical area,- -

In claim 20, between lines 10 and 11, insert:

- -predicting yield of integrated circuit devices produced from said integrated circuit design based on said critical area,- -

(This Examiner's amendment has been made in order to place the application in a condition for allowance)

Reasons for Allowance

3. The following is an examiner's statement of reasons for allowance:

4. Claim 4 is allowed because the prior art made of record does not teach or suggest:

A method of determining critical areas associated with different types of fault mechanisms in an integrated circuit design, said method comprising:

constructing individual Voronoi diagrams for critical areas of individual fault mechanisms;

constructing a composite Voronoi diagram based on said individual Voronoi diagrams;

computing the critical area for composite fault mechanisms of said integrated circuit design based on said composite Voronoi diagram; and

predicting yield of integrated circuit devices produced from said integrated circuit design based on said critical area,

wherein said constructing of said composite Voronoi diagram comprises constructing a three dimensional representation of critical area for said composite fault mechanism.

5. Claim 6 is allowed because the prior art made of record does not teach or suggest:

A method of determining critical areas associated with different types of fault mechanisms in an integrated circuit design, said method comprising:

constructing individual Voronoi diagrams for critical areas of individual fault mechanisms;

constructing a composite Voronoi diagram based on said individual Voronoi diagrams;

computing the critical area for composite fault mechanisms of said integrated circuit design based on said composite Voronoi diagram; and

predicting yield of integrated circuit devices produced from said integrated circuit design based on said critical area,

wherein said constructing of said composite Voronoi diagram comprises forming a logical AND composite of said individual fault mechanisms.

6. Claim 7 is allowed because the prior art made of record does not teach or suggest:

A method of determining critical areas associated with different types of fault mechanisms in an integrated circuit design, said method comprising:

constructing individual Voronoi diagrams for critical areas of individual fault mechanisms;

constructing a composite Voronoi diagram based on said individual Voronoi diagrams;

computing the critical area for composite fault mechanisms of said integrated circuit design based on said composite Voronoi diagram; and

predicting yield of integrated circuit devices produced from said integrated circuit design based on said critical area,

wherein said constructing of said composite Voronoi diagram comprises forming a logical NOT of said individual fault mechanisms.

7. Claim 10 is allowed because the prior art made of record does not teach or suggest:

A method of determining critical areas associated with different types of fault mechanisms in an integrated circuit design, said method comprising:

constructing individual Voronoi diagrams for critical areas of individual fault mechanisms;

constructing a logical OR composite Voronoi diagram of said individual Voronoi diagrams;

computing the critical area for composite fault mechanisms of said integrated circuit design based on said composite Voronoi diagram; and

predicting yield of integrated circuit devices produced from said integrated circuit design based on said critical area,

wherein said constructing of said composite Voronoi diagram comprises constructing a three dimensional representation of critical area for said composite fault mechanism.

8. Claim 11 is allowed because the prior art made of record does not teach or suggest:

A method of determining critical areas associated with different types of fault mechanisms in an integrated circuit design, said method comprising:

constructing individual Voronoi diagrams for critical areas of individual fault mechanisms;

constructing a logical OR composite Voronoi diagram of said individual Voronoi diagrams;

computing the critical area for composite fault mechanisms of said integrated circuit design based on said composite Voronoi diagram; and

predicting yield of integrated circuit devices produced from said integrated circuit design based on said critical area,

further comprising computing the critical area of a logical NOT of said individual fault mechanisms in a process comprising subtracting the critical area of said individual fault mechanisms from the area of said integrated circuit.

9. Claim 12 is allowed because the prior art made of record does not teach or suggest:

A method of determining critical areas associated with different types of fault mechanisms in an integrated circuit design, said method comprising:

constructing individual Voronoi diagrams for critical areas of individual fault mechanisms;

constructing a logical OR composite Voronoi diagram of said individual Voronoi diagrams;

computing the critical area for composite fault mechanisms of said integrated circuit design based on said composite Voronoi diagram; and

predicting yield of integrated circuit devices produced from said integrated circuit design based on said critical area,

further comprising computing the critical area of a logical AND of said individual fault mechanisms in a process comprising:

adding the critical areas of a first individual fault mechanism to a second individual fault mechanism to produce an intermediate result; and

subtracting the critical area of said logical OR composite of said first individual fault mechanism and said second individual fault mechanism from said intermediate result.

10. Claim 13 is allowed because the prior art made of record does not teach or suggest:

A method of determining critical areas associated with different types of fault mechanisms in an integrated circuit design, said method comprising:

constructing individual Voronoi diagrams for critical areas of individual fault mechanisms;

constructing a logical OR composite Voronoi diagram of said individual Voronoi diagrams;

computing the critical area for composite fault mechanisms of said integrated circuit design based on said composite Voronoi diagram; and

predicting yield of integrated circuit devices produced from said integrated circuit design based on said critical area,

further comprising computing the critical area of any boolean composition of said individual fault mechanisms in a process comprising:

arranging the boolean composition into disjunctive normal form; and

computing the sums and differences of component critical areas of logical OR composites of subsets of said individual fault mechanisms.

11. Claim 18 is allowed because the prior art made of record does not teach or suggest:

A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method of determining critical areas associated with different types of fault mechanisms in an integrated circuit design, said method comprising:

constructing individual Voronoi diagrams for critical areas of individual fault mechanisms;

constructing a composite Voronoi diagram based on said individual Voronoi diagrams;

computing the critical area for composite fault mechanisms of said integrated circuit design based on said composite Voronoi diagram; and

predicting yield of integrated circuit devices produced from said integrated circuit design based on said critical area,

wherein said constructing of said composite Voronoi diagram comprises constructing a three dimensional representation of critical area for said composite fault mechanism.

12. Claim 20 is allowed because the prior art made of record does not teach or suggest:

A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method of determining critical areas associated with different types of fault mechanisms in an integrated circuit design, said method comprising:

constructing individual Voronoi diagrams for critical areas of individual fault mechanisms;

constructing a composite Voronoi diagram based on said individual Voronoi diagrams;

computing the critical area for composite fault mechanisms of said integrated circuit design based on said composite Voronoi diagram; and

predicting yield of integrated circuit devices produced from said integrated circuit design based on said critical area,

wherein said constructing of said composite Voronoi diagram comprises forming a logical AND composite of said individual fault mechanisms.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul Dinh

PAUL DINH
PRIMARY EXAMINER

Suchin Parihar
Examiner
AU 2825